PRODUCT SPECIFICATION

MODEL NO: SEL37100-DT024QV

< > PRELIMINARY SPECIFICATION

< > APPROVAL SPECIFICATION

CUSTOMER
APPROVED BY
DATE:

DESIGNED	CHECKED	APPROVED

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RECORDS OF REVISION

REV.	DATE	Page	DESCRIPTION OF CHANGES
01	2011.3.31		FIRST ISSUE

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CONTENT

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1. GENERAL SPECIFICATION

1.1 Description

The SEL97100-DT024QV is a color active matrix Thin Film Transistor (TFT) Liquid Crystal Display (LCD) that uses amorphous silicon(a-Si) TFT as a switching device. This model is composed of a single 2.4 inches transmissive type main TFT-LCD panel. The resolution of the panel is 240x320 pixels and can display up to 262K color.

1.2 Feature

-TM type for main TFT-LCD panel
-Structure COG+FPC+BL
-Full, Normal (Still), Partial, Sleep, Standby mode are available

1.3 Application

-Display terminals for cellular phone

1.4 General Specification

No.	Item	Specification	Unit	Remark
1	LCD Size	2.4	inch	-
2	Panel Type	a-Si TFT active matrix	-	-
3	Resolution	240 x (RGB) x 320	pixel	-
4	Display Mode	Normally white,Transmissive	-	-
5	Display Number of Colors	262K	-	-
6	Viewing Direction	12 o'clock(Peak CR) /6 o'clock(Good View)	-	Note
7	Contrast Ratio	300(Typ)	-	-
8	Luminance	300(Typ)	cd/m^2	-
9	Module Size	41.52(W) x 59.16(L) x 2.5(T)	mm	Note
10	Active Area	36.72(W) x 48.96(L)	mm	Note
11	Pixel Pitch	0.153(W) x 0.153(L)	mm	-
12	Weight	TBD(TYP)	g	-
13	Driver IC	HX8347D	-	-
14	Driver IC RAM Size	240x18x320	bit	-
15	Light Source	4 LEDs White	℃	-
16	Interface	80-system 8bit Parallel/SPI	℃	-
17	Operating Temperature	-20~70		-
18	Storage Temperature	-30~80		-

Note: Please refer to the mechanical drawing.

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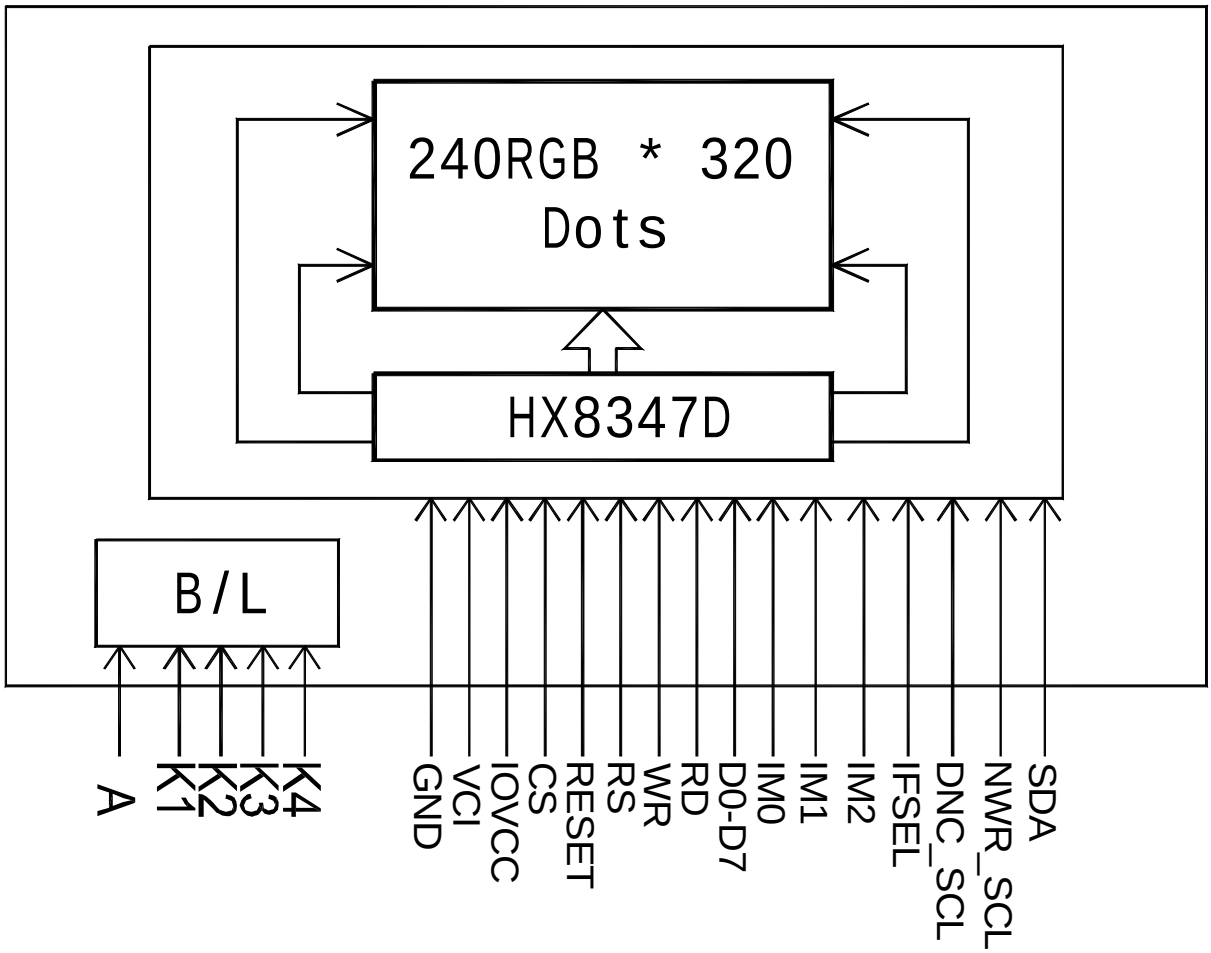
2. BLOCK DIAGRAM



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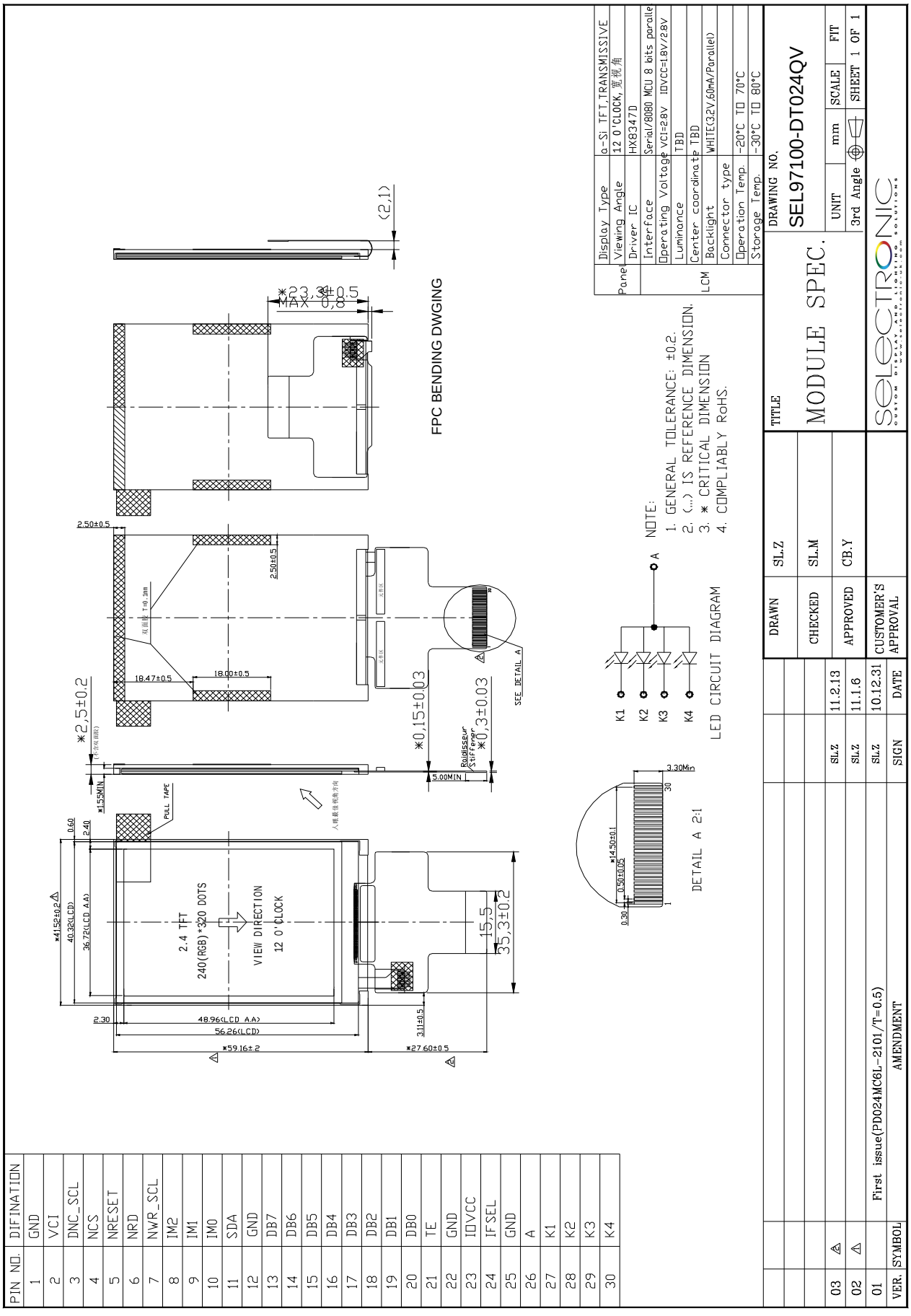
3. MECHANICAL DRAWING



PIN NO.	DIFINATION
1	GND
2	VCI
3	DNC_SCL
4	NCS
5	NRESET
6	NRD
7	NWR_SCL
8	IM2
9	IM1
10	IM0
11	SDA
12	GND
13	DB7
14	DB6
15	DB5
16	DB4
17	DB3
18	DB2
19	DB1
20	DB0
21	TE
22	GND
23	IOVCC
24	IFSEL
25	GND
26	A
27	K1
28	K2
29	K3
30	K4

Panel	Display Type	a-Si TFT,TRANSMISSIVE
	Viewing Angle	12 O'CLOCK, 宽视角
	Driver IC	HX8347D
	Interface	Serial/8080 MCU 8 bits parallel
LCM	Operating Voltage	VCI=2.8V IOVCC=1.8V/2.8V
	Luminance	TBD
	Center coordinate	TBD
	Backlight	WHITE(3.2V,60mA/Parallel)
	Connector type	
	Operation Temp.	-20°C TO 70°C
	Storage Temp.	-30°C TO 80°C

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4. INTERFACE ASSIGNMENT

PIN NO.	FUNCTION DESCRIPTIONS	SYMBOL
1	Connect to GND	GND
2	Analog power supply	VCI
3	(DNC) Command / parameter or display data selection pin. (SCL) server as serial data clock in serial bus system interface when IFSEL=1.	DNC_SCL
4	Chip select signal.	NCS
5	RESET signal	NRESET
6	Read enable pin I80 parallel bus system interface.	NRD
7	(NWR) Write enable pin I80 parallel bus system interface. (SCL) server as serial data clock in serial bus system interface	NWR_SCL
8	System interface select.	IM2
9		IM1
10		IM0
11	Serial data input pin and output pin in serial bus system interface. The data is inputted on the rising edge of the SCL signal.	SDA
12	Connect to GND	GND
13	Data Bus	DB7
14		DB6
15		DB5
16		DB4
17		DB3
18		DB2
19		DB1
20		DB0
21	Tearing effect output.	TE
22	Connect to GND	GND
23	Digital IO pad power	IOVCC
24	Interface format select pin	IFSEL
25	Connect to GND	GND
30	B/L LED+	A
31	B/L LED-	K1
32	B/L LED-	K2
33	B/L LED-	K3
34	B/L LED-	K4

1,System interface select.(the IFSEL has to be connected to GND)

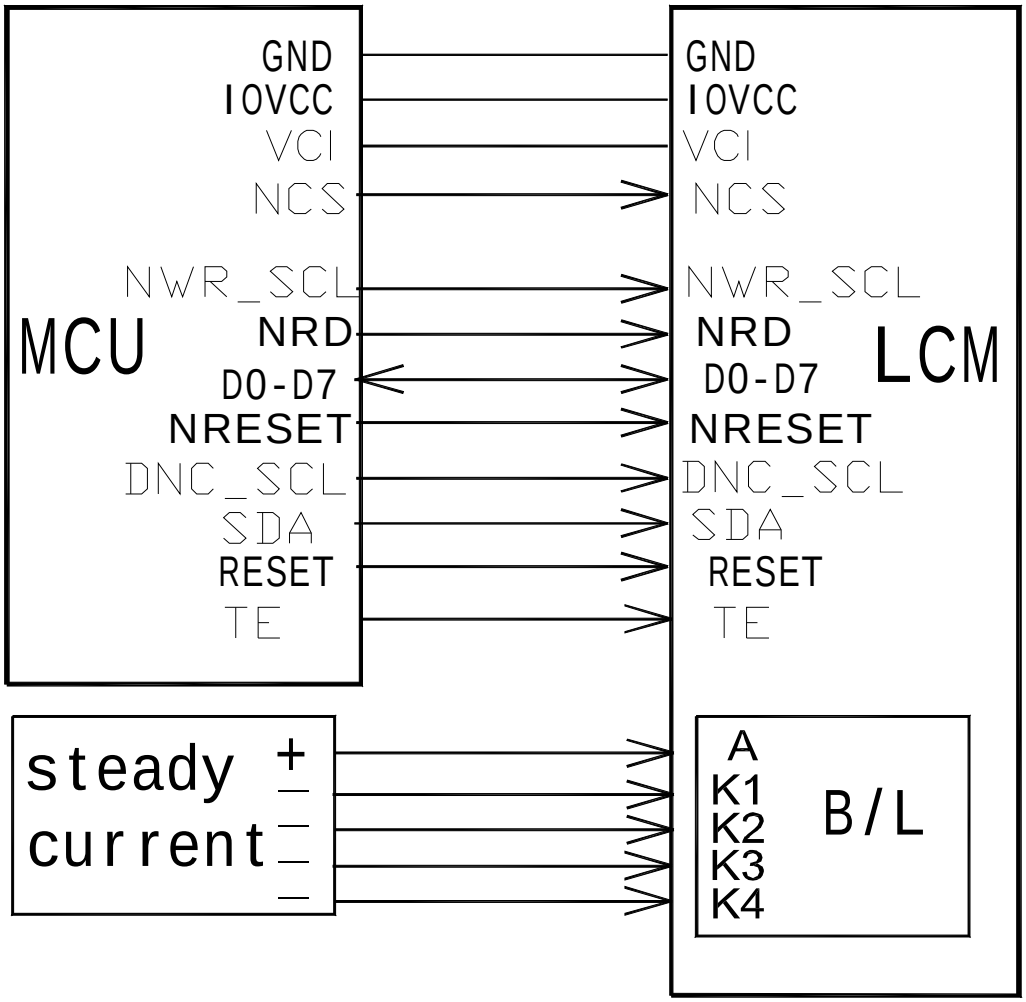
IM0	IM1	IM2	interface
0	1	1	8080 MCU 8-bit parallel [D7-D0]
1	0	ID	3-wire serial interface
1	1	-	4-wire serial interface

2,Interface format select pin.

IFSEL	Interface Format Selection
0	Register-content interface mode
1	Command-Parameter interface mode

5. ELECTRICAL SPECIFICATION

5.1. APPLICATION CIRCUIT



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5.2. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	V_{CI}	Ta=25 ºC	2.3	-	3.3	V
Power Supply for Digital IO	IOV_{CC}	Ta=25 ºC	1.65	-	3.3	V

Note: Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is applied.

5.3. TYPICAL OPERATION CONDITION

5.3.1 DC Characteristics

ITEM	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
Power Supply for Analog	V_{CI}	Ta=25 ºC	2.3	2.8	3.3	V
Power Supply for Digital IO	IOV_{CC}	Ta=25 ºC	1.65	1.8	3.3	V
Input Signal “H” Level	V_{IH}	-	$0.7V_{CC2}$	-	V_{CC2}	V
Input Signal “L” Level	V_{IL}	-	-0.3	-	$0.3V_{CC2}$	V
Output Signal “H” Level	V_{OH}	I_{OH}=-0.1mA	$0.8V_{CC2}$	-	-	V
Output Signal “L” Level	V_{OL}	I_{OL}=0.1mA	-	-	$0.2V_{CC2}$	V
Frame Frequency	f_{FRAME}	-	-	60	-	Hz

Note: To prevent IC latch up or DC operation in LCD panel, the power on/off sequence should follow the driver IC specification.

5.3.2 Current Consumption

Item	Symbol	Values		Unit	Remark
		Typ.	Max.		
80-system 8-bit parallel Interface					
Normal(Still) Mode	I_{CC1}	4.5	9.0	mA	Note1
Sleep Mode	I_{CC2}	--	50	uA	Note2

Note1: Test Condition

IOVCC=VCI=2.8V;

Display Pattern: 8 Color Bar

Frame Rate=60Hz at Line Inversion

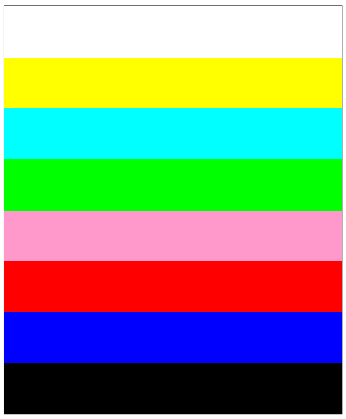
Operating Temperature: 25℃

Display Pattern: All Pixel Black

Frame Rate=60Hz at Line Inversion

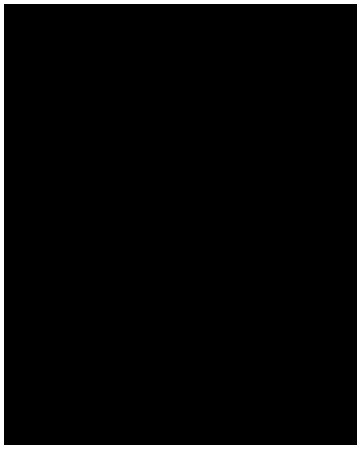
Operating Temperature: 25℃

Typ. current check pattern:



8-Color Bar

Max. current check pattern:



Black

Note2: In the standby mode, all the internal display operations are suspended including the internal R-C oscillator.

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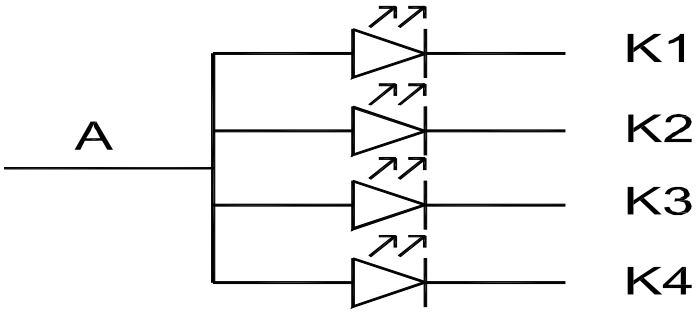
5.4.1 BACKLIGHT CIRCUIT



5.4.2 ELECTRICAL CHARACTERISTICS (T=25℃)

PARAMETER	SYMBOL	CONDITION	STANDARD VALUE			UNIT
			MIN	TYP	MAX	
FORWARD VOLTAGE (Single Chip)	VF	IF=15mA	2.9	3.2	3.4	V

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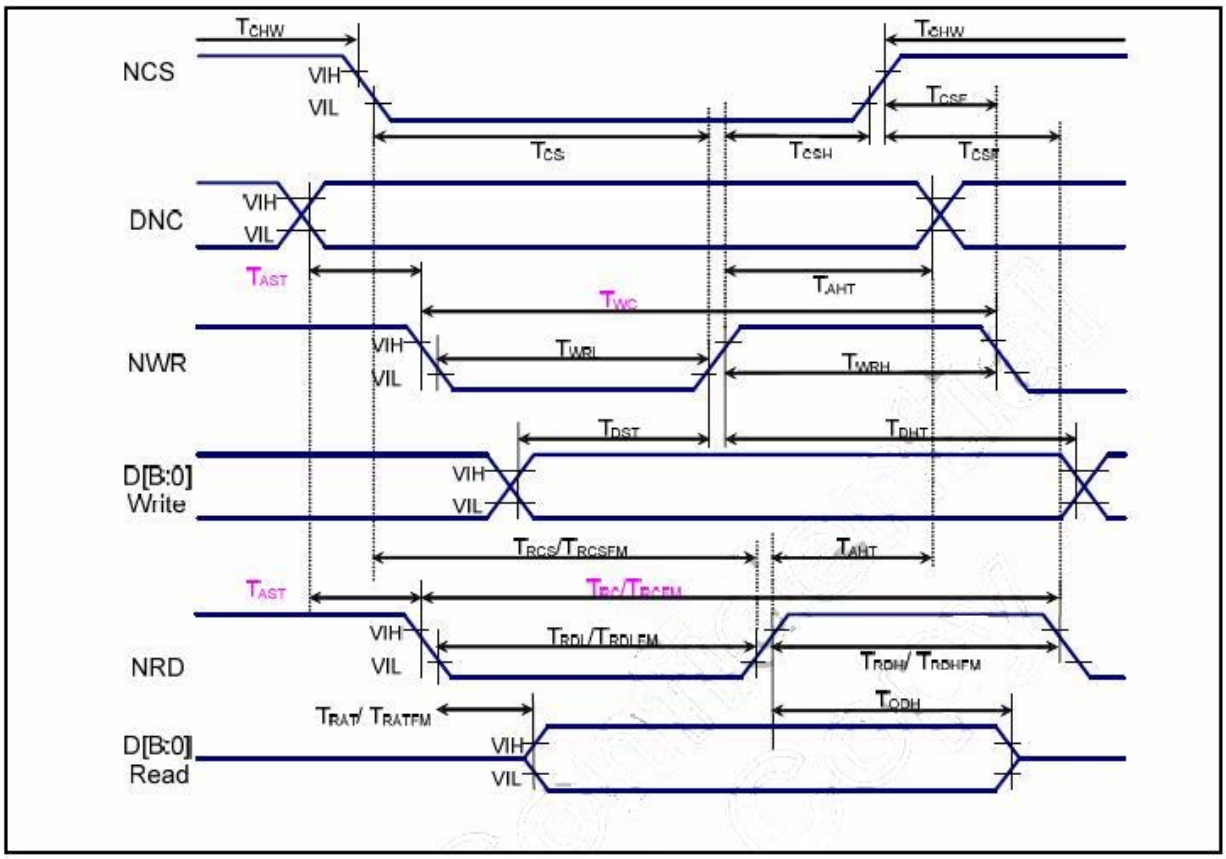
5.5. INTERFACE TIMING CHARACTERISTICS



5.6.

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70° C)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
DNC_SCL	tAST	Address setup time	0	-	ns	-
	tAHT	Address hold time (Write/Read)	10	-		
NCS	tCHW	Chip select "H" pulse width	0	-	ns	-
	tCS	Chip select setup time (Write)	15	-		
	tRCS	Chip select setup time (Read ID)	45	-		
	tRCSFM	Chip select setup time (Read FM)	355	-		
	tCSF	Chip select wait time (Write/Read)	10	-		
	tCSH	Chip select hold time	10	-		
NWR_SCL	tWC	Write cycle	66	-	ns	-
	tWRH	Control pulse "H" duration	15	-		
	tWRL	Control pulse "L" duration	15	-		
NRD(ID)	tRC	Read cycle (ID)	160	-	ns	When read ID data
	tRDH	Control pulse "H" duration (ID)	90	-		
	tRDL	Control pulse "L" duration (ID)	45	-		
NRD(FM)	tRCFM	Read cycle (FM)	450	-	ns	When read from frame memory
	tRDHFM	Control pulse "H" duration (FM)	90	-		
	tRDLFM	Control pulse "L" duration (FM)	355	-		
DB17 to DB0	tDST	Data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tDHT	Data hold time	10	-		
	tRAT	Read access time (ID)	-	40		
	tRATFM	Read access time (FM)	-	340		
	tODH	Output disable time	20	80		

Note: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

RESET TIMING CHARACTERISTICS

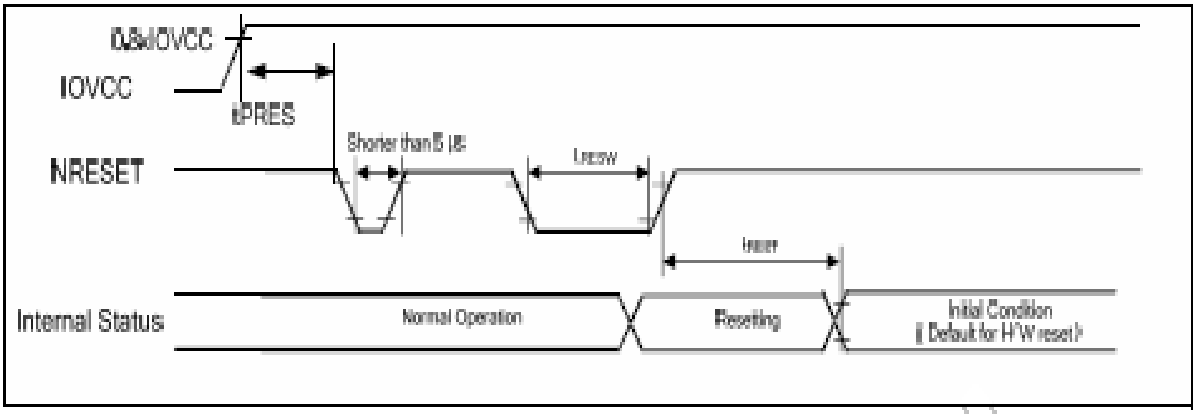


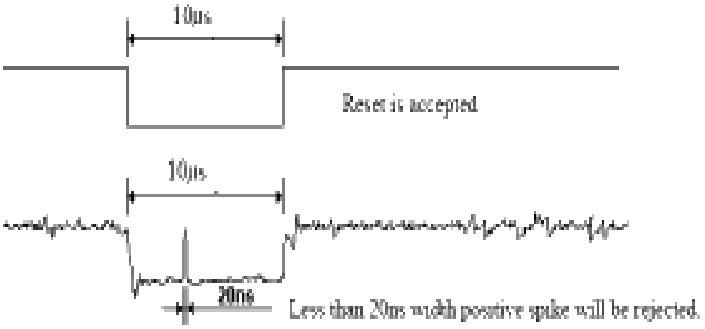
Figure 11.5 Reset input timing

Symbol	Parameter	Related Pins	Spec. Min.	Spec. Typ.	Spec. Max.	Note	Unit
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	μs
tREST	Reset complete time(2)	-	-	-	5	When reset applied during STB OUT mode	ms
		-		-	120	When reset applied during STB mode	ms
tPRES	Reset goes high level after Power on time	NRESET & IOVCC	1	-	-	Reset goes high level after Power on	ms

Note: (1) Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the table below.

NRESET Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in STB Out –mode. The display remains the blank state in STB –mode) and then return to Default condition for H/W reset.
(3) During Reset Complete Time, VMF value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of NRESET.
(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) It is necessary to wait 5msec after releasing !RES before sending commands. Also STB Out

6. OPTICAL CHARACTERISTICS

(T_a=+25°C,VCI=IOVCC=+2.8V,I_{BI}=60mA)

Item		Symbol	Condition	Values			Unit	Remark
				Min.	Typ.	Max.		
Viewing Angle Range	Left	θ_L	CR≧10	50	60	-	degree	Note 1,2
	Right	θ_R		50	60	-		
	Top	Φ_T		55	65	-		
	Bottom	Φ_B		40	50	-		
Response Time		T_{on} +T_{off}	Normal θ=Φ=0°	-	30	60	ms	Note 2,3
Contrast Ratio		CR	Normal θ=Φ=0°	200	300	-	-	Note 2,4
Luminance		L	Normal θ=Φ=0°	270	300	--	cd/m^2	Note 2,5
Color Chromaticity (CIE1931)	White	W_x	Normal θ=Φ=0°	0.226	0.276	0.326	-	Note 2,6
		W_y		0.238	0.288	0.338		
	Red	R_x		0.523	0.573	0.623		
		R_y		0.283	0.333	0.383		
	Green	G_x		0.285	0.335	0.385		
		G_y		0.540	0.590	0.640		
	Blue	B_x		0.096	0.146	0.196		
		B_y		0.007	0.057	0.107		
Color Gamut		NTSC	CIE1931	-	50	-	%	-
Luminance Uniformity		U_L	Normal θ=Φ=0°	75	80	-	%	Note 2,7

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Note 1: Definition of viewing angle range

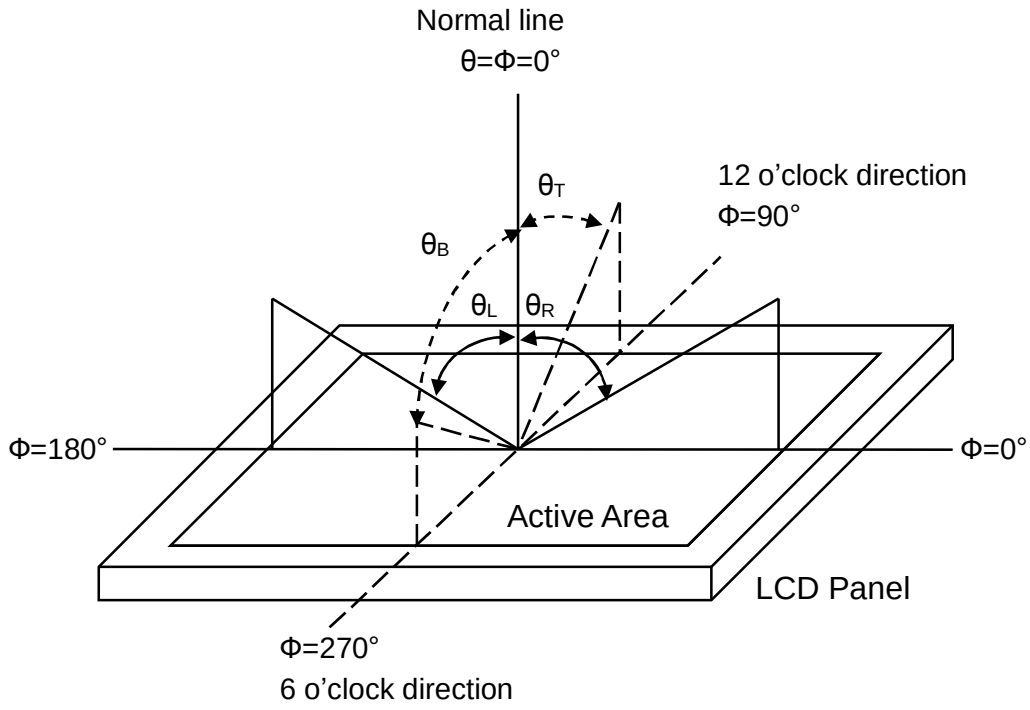

Fig. 1 Definition of viewing angle

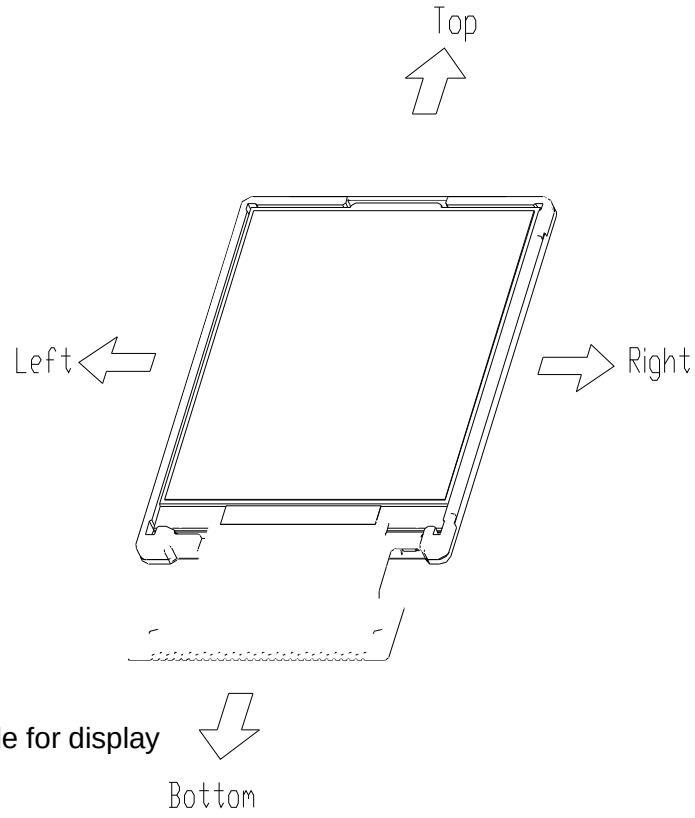

Fig. 2 Definition of viewing angle for display

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Note 2: Definition of optical measurement system

The optical characteristics should be measured in a dark room with ambient temperature T_a=+25 . The optical properties are measured at the center point of the LCD screen after 5 minutes operation. (Equipment: Photo detector TOPCON BM-5AS Field of view: 1°/Height: 500mm.)

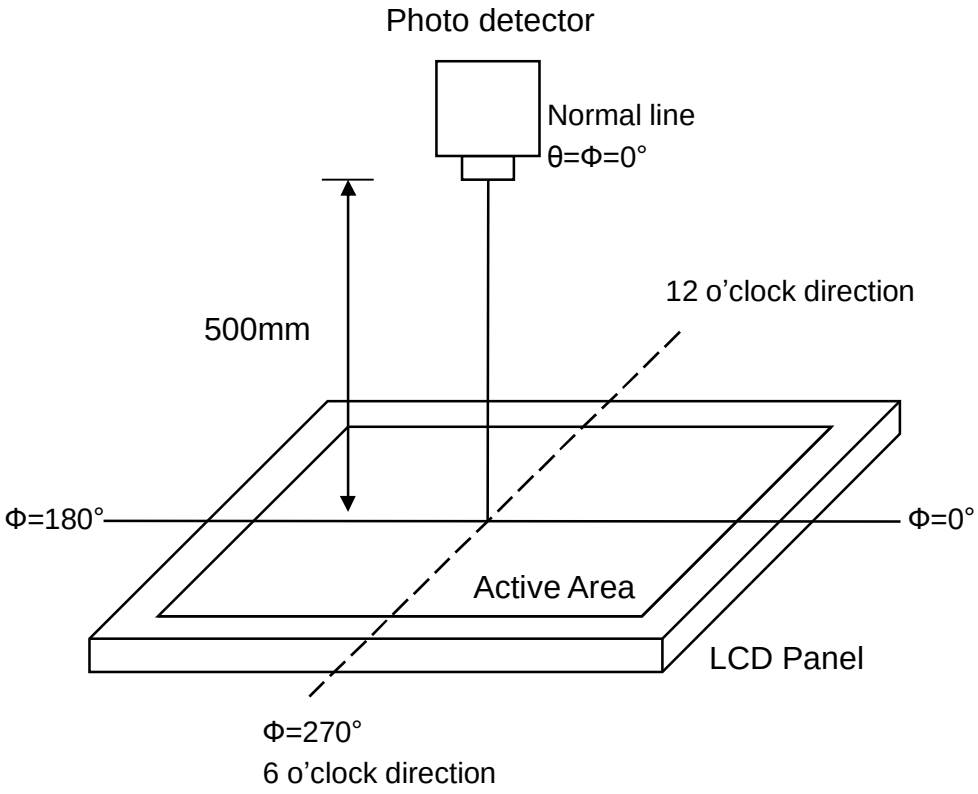
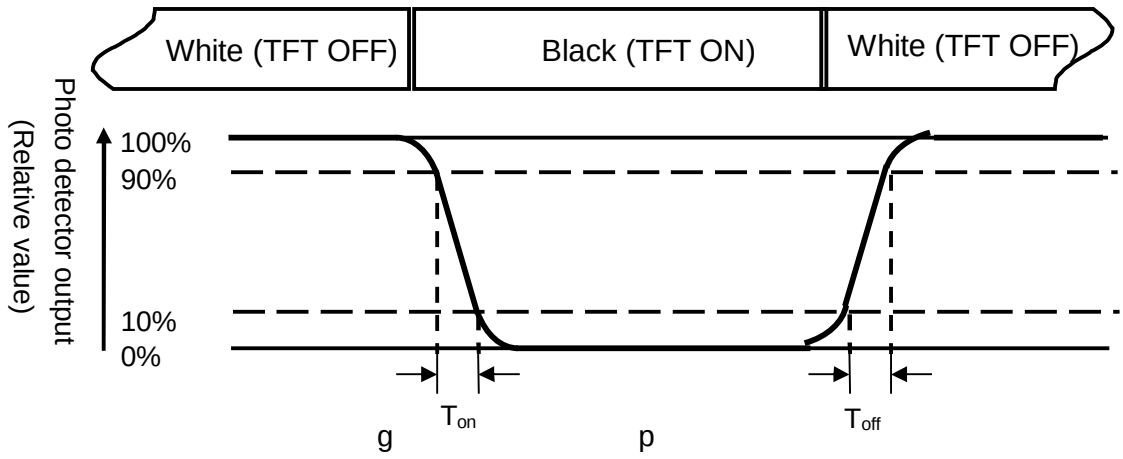


Fig. 3 Optical measurement system setup

Note 3: Definition of response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (T_{on}) is the time between photo detector output intensity changed from 90% to 10%, and fall time (T_{off}) is the time between photo detector output intensity changed from 10% to 90%.



g p

Fi . 4 Definition of res onse time

Note 4: Definition of contrast ratio

$$\text{Contrast ratio (CR)} \quad \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note 5: Definition of luminance

Measured at the center area of the panel when LCD panel is driven at “white” state.

Note 6: Definition of color chromaticity (CIE1931)

Color coordinates measured at the center point of LCD when panel is driven at “White”, “Red”, “Green” and “Blue” state respectively.

Note 7: Definition of luminance uniformity

To test for uniformity, the tested area is divided into 3 rows and 3 columns. The measurement spot is placed at the center of each circle as below.

$$\text{Luminance Uniformity } (U_L) = \frac{L_{min}}{L_{max}}$$

L-------Active area length W----- Active area width

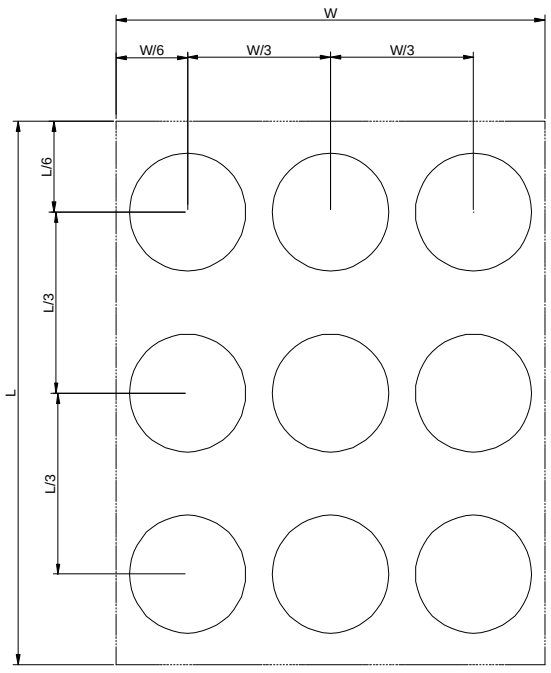


Fig. 5 Definition of luminance uniformity

L_{min} : The measured minimum luminance of all measurement position.

L_{max} : The measured maximum luminance of all measurement position.

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7. RELIABILITY TESTS

ITEM	CONDITION	CRITERION
Operating Temperature Test	High Temperature: +70 ºC±3℃, 72 hrs	No defects in display and operational functions
	Low Temperature: -20 ºC±3℃, 72 hrs	
Storage Temperature Test	High Temperature: +80 ºC±3℃, 120 hrs	No defects in display and operational functions
	Low Temperature: -30 ºC±3℃, 120 hrs	
Humidity Endurance Test	60 ºC±3℃, 90%±3%RH, 72 hrs	No defects in display and operational functions
Thermal Shock Test	-30 ºC (30mins)～ +80 ºC (30mins) 10 cycles	No defects in display and operational functions
Vibration Resistance Test	Operating Time: thirty minutes exposure for each direction (X,Y,Z) Sweep Frequency:10~55Hz (1 min) Amplitude: 1.5mm	No defects in display and operational functions
Mechanical Shock	100G 6ms,±X, ±Y, ±Z 3 times for each direction	No defects in display and operational functions
Package Vibration Test	Random Vibration : $0.015G^2$/Hz from 5-200Hz, -6dB/Octave from 200-500Hz 1 hour for each direction of X. Y. Z. (3 hours for total)	No defects in display and operational functions
Package Drop Test	Height :72cm(Weight≦10kg); 60cm(Weight≧10kg) 1 corner, 3 edges, 6 surfaces	No defects in display and operational functions
Electro Static Discharge	± 2KV, Human Body Mode, 100pF/1500Ω	No defects in display and operational functions

NOTE:

1) The samples must be free from defect before test, must be restored at room condition at least for 2 hours after reliability test before any inspection.

2) Before test the function of TP, the sample must be placed in room temperature for 24hrs after RA test.

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8 PRECAUTIONS

8.1. HANDLING

8.1.1. Polarizer Cleaning, Petroleum ether (or N-hexane) is recommended for cleaning the front/rear polarizers and reflectors, acetone, toluene and ethanol are not allowed to avoid damaging the surface.

8.1.2. Body grounding, must wear Anti-ESD wrist strap while pick up LCDs.

8.1.3. FPC Soldering, less than 300 /3S, solder must be grounding on grounding bench.

8.1.4. If use electric Screwdriver to do assembly, screwdriver must be grounding.

8.2. STORAGE

8.2.1. Keep in a sealed polyethylene bag.

8.2.2. Keep in a dark place.

8.2.3. Keep in temperature between 0 ° C and 35 ° C.

NOT allowed at 70 ° C for more than 160 Hours, or at -20 ° C for more than 48 Hrs.

8.3. SAFETY

If liquid crystal leak out of a damaged glass cell, **DO NOT** put it in your mouth or touch eyes, if the liquid crystal touch your skin or clothes, please wash it off immediately using soap and water.

9. LIMITED WARRANTY

Unless otherwise agreed between the factory and customer, the factory will replace or repair any of it's LCD modules which are found to be functionally defective when inspected in accordance with the factory LCD acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects over specs must to be returned to the factory within 30 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of the factory to repair and/or replacement on the terms set forth above. The factory shall not be responsible for any subsequent or consequential events.

9.1. RETURNING LCM UNDER WARRANTY TERMS AND CONDITIONS

9.1.1. No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- Circuit modified in any way, including addition of components.

9.1.2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB's eyelet, conductors and terminals.